REMARKS

Applicants sincerely appreciate the continued thorough examination of the present application as evidenced by the Office Action of August 14, 2009. In response, Applicants have: amended Claim 8; cancelled Claims 10-11; presented new claims 21-23 which correspond to previously presented claims 9-11; and presented new claims 24-33. Applicants respectfully submit that these claims are patentable over the cited references for at least the reasons discussed below.

Applicants further appreciate the Examiner's courtesy in conducting a telephonic interview with the undersigned attorney on October 20, 2009. In the interview, the parties discussed the claim amendments shown above. No agreement was reached. Applicants respectfully submit that the above remarks constitute an Interview Summary pursuant to MPEP §713.04.

In the Office Action, Claims 8 and 10-12 were rejected under 35 USC § 103(a) as unpatentable over U.S. Patent No. 7,065,036 to Ryan in view of JP 2001-022731 to Makato. Office Action at 2.

Applicants respectfully submit that Claim 8, as amended, is patentable over Ryan in view of Makato, as neither of these references appears to disclose or suggest buffering first data having a length of N/2 and simultaneously transforming the first data and second data having a length of N/2 using an N-point FFT processor as the second data is received. For example, although Makato discloses pipeline FFT processing of data from two N/2 input data pairs stored in two N/2 sized memories, both of the N/2 input data pairs are buffered in the memory. Ryan achieves increased throughput by increasing the sample processing rate when all samples have entered the pipeline. Thus, both references operate on different principles from the invention as recited in Claim 8.

As amended, Claim 8 recites (emphasis added):

> 8. A method of transforming an Orthogonal Frequency Division Multiplexing (OFDM) signal by a fast Fourier transform (FFT) processor, the OFDM signal having a symbol, the symbol including a preamble and first data following the preamble, the preamble having a sequence of N-samples and the first data having a sequence of N/2 samples, the method comprising:
>
> storing the preamble in a memory as the OFDM signal is received;

reading the preamble from the memory in response to an end point of the preamble being detected, transforming the preamble by a fast Fourier transform into a transformed preamble, and storing the transformed preamble in the memory;

buffering first data that follows the preamble while the preamble is transformed;

simultaneously transforming second data that is received by the FFT processor after the first data is buffered and that has a sequence of N/2 samples, and the buffered first data, respectively, using an N-point FFT transform into third data as the second data is received, and

storing the third data in the memory, and outputting the third data.

Applicants respectfully submit that Ryan in view of Makato do not disclose or suggest at least the underlined recitations of Claim 8. FFT processing of data in this manner can reduce or eliminate data delay that occurs due to input buffering in conventional OFDM systems. As explained in the Specification of the present application:

> [0069] Referring to FIGS. 7 and 8, the memory bank 223 allows an average of the long preambles T1 and T2 to be completely input to the radix-2 FFT during an N/2 clock cycle after timing acquisition occurs. The memory bank 223 functions as an output memory after the average of the long preambles is completely input to the radix-2 FFT. The first half data of the data is stored in the FFT input buffer 221 after the symbol is input to the into the radix-2 FFT 222, and the latter half data of the input data is input into the radix-2 FFT 222 as soon as the latter half data is input. Accordingly, the delay due to input buffer may be reduced or eliminated according to embodiments of the present invention.

Specification, para. [0069] (emphasis added). Stated differently, after the average of the long preambles T1 and T2 is input, the first N/2 samples of the data symbol are stored in an FFT input buffer. Then, the FFT data are processed as the second N/2 samples of the data symbol (i.e., the latter half data) are received.

Ryan discloses a radio receiver configured to perform OFDM processing. Ryan, Abstract, and col. 4, lines 4-9. According to Ryan, OFDM samples are provided to a processing pipeline. Ryan, Abstract. The processing pipeline processes samples at a first clock rate until it is determined that all samples have entered the pipeline, at which point the processing pipeline processes the sample at a second, higher rate. Ryan, Abstract. Accordingly, Ryan obtains increased processing throughput by changing the processing rate

of samples. Ryan does not disclose or suggest "simultaneously transforming second data that is received by the FFT processor after the first data is buffered and that has a sequence of N/2 samples, and the buffered first data, respectively, using an N-point FFT transform into third data as the second data is received."

Makato discloses a fourier transform unit that operates according to a butterfly operation. Makato, para. [0001]. Makato discloses pipeline FFT processing of data from two N/2 input data pairs stored in two N/2 sized memories, both of the N/2 input data pairs are buffered in the memory.

The Office Action cites paragraph [0006] of Makato as disclosing FFT processing of first half and second half data of an OFDM symbol. However, Makato appears to describe that both the first half and second half data are already buffered before FFT processing is performed thereon. For example, Makato para. [0006] states that both first and second input buffers are used, each of which can store N/2 samples of data. Makato appears to disclose that "Begin to read one data at a time from the 1st and 2nd input buffers, and it inputs into a butterfly computing unit, It writes at a time two data [one] which is an operation result from this butterfly computing unit in the 1st and 2nd memories." Makato, para [0006]. That is, Makato appears to disclose that N/2 samples of the data that is being operated on are stored in a first input buffer and N/2 samples are stored in a second input buffer. Data is drawn from the input buffers and processed by a butterfly processor.

Accordingly, neither Ryan nor Makato discloses or suggests at least "buffering first data that follows the preamble while the preamble is transformed" and "simultaneously transforming second data that is received by the FFT processor after the first data is buffered and that has a sequence of N/2 samples, and the buffered first data, respectively, using an N-point FFT transform into third data as the second data is received" as recited in Claim 8.

Claim 28 recites an FFT processor including "an FFT input buffer that is configured to store the N/2 samples of the first data while the preamble is being transformed, wherein the signal converter is further configured to perform an N-point FFT of the buffered first data and second data having a sequence of N/2 samples as the second data is sequentially received to transform the first data and the second data into third data having N samples." Accordingly, Claim 28 is believed to be patentable over Ryan in view of Makato for at least similar reasons as Claim 8.

The dependent claims are patentable at least based on the patentability of the independent claims.

CONCLUSION

In light of the foregoing amendments, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,
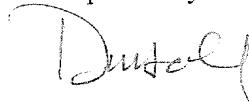
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